Wideband Distributed Choke Inductor for Distributed Power Amplifiers

Çağdaş Ballı, Ahmet Değirmenci, Ahmet Aktuğ, and Abdullah Atalar, *Fellow, IEEE*

***Abstract*—A method to design a wideband, low-loss, and high-current choke inductor suitable for use in a distributed power amplifier (DPA) is presented. The choke inductor is composed of several parallelled low-current inductors with small parasitics placed in a distributed manner. High-frequency gain limiting parasitic shunt capacitors of these inductors are absorbed by the series inductors already present between the transistor drain terminals of the distributed amplifier. The measurement results of a 2–18 GHz DPA designed using a distributed choke inductor with an equivalent DC resistance of 0.32 Ω are given.**

***Index Terms*—distributed power amplifier, non-uniform distributed power amplifier, choke inductor, MMIC, GaN.**

I. Introduction

WIDEBAND solid-state amplifiers are usually based on the distributed amplifier topology. To improve output power and power-added efficiency, the non-uniform distributed power amplifier (NDPA) topology using a GaN-based process is typically used [1]. This topology provides high output power and enhanced efficiency over a large bandwidth. Various GaN MMIC NDPAs were proposed to obtain the maximum achievable output power in the frequency range of 2–18 GHz [2, 3, 4, 5, 6].

One of the factors that limits the performance of an NDPA is the drain bias choke inductor. It must be able to handle the high supply current while keeping its series resonance frequency out of the band, and have a sufficiently high inductance to provide adequate impedance at the bottom of the band. Moreover, it should have small shunt parasitics not to limit the performance at high frequencies.

Conical inductors as discrete components with high series resonance frequencies are commercially available. However, their use as off-chip inductors is problematic due to the band-limiting effect of the bonding pad capacitance at the drain line.

Using an on-chip wideband small-size 1:4 Ruthroff output impedance transformer is very advantageous since one can design for a four times lower drain-side impedance to improve the output power and reduce the value of the on-chip choke inductor [7], [8], by the same factor. An on-chip LC branch [9] is needed for the transformation at low frequencies, through which DC drain bias current is supplied.

In many cases, the amplifier bandwidth is determined by the parasitics of the bias choke inductor and not the frequency capability of the core NDPA [10]. This article presents a method to design a wideband, low-loss, and high-current choke inductor suitable for distributed power amplifiers.

An on-chip circular spiral inductor is often used as a drain bias choke in distributed power amplifiers because of its large bandwidth and relatively small size. However, high-current spiral inductors tend to have large shunt parasitics degrading the performance at high frequencies. In the next section, the series resonance frequency and the parasitic components of this inductor are characterized. In Section III, we introduce the distributed choke inductor with eliminated parasitic shunt capacitors that can be realized on a small chip area. Section IV presents the measurement results of an NDPA containing the proposed distributed choke inductor.

II. Spiral Inductor

Several spiral inductors optimized with EM simulations are fabricated using a 0.25μm GaN on SiC process[1], one of which is shown in Fig. 1, where air bridges are used to connect to the

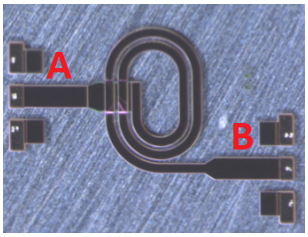

Fig. 1: A spiral inductor fabricated with a 0.25 μm process.

center of the inductor. Two-port S-parameter measurements are carried out for full characterization of inductors. Subsequently, inductors are simulated in a bias-tee configuration [2] with one port shorted to ground as depicted in Fig. 2.

A lumped element circuit model for a circular spiral inductor is shown in Fig. 3 [11], where L_c is the total inductance

[1]Win Semiconductors Corp., Taiwan.

[2]Inductor manufacturers prefer the bias-tee configuration to demonstrate their choke inductors intended for biasing an amplifier.

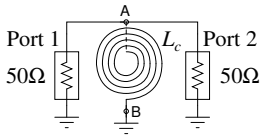

Fig. 2: Method of characterization for a spiral inductor

Çağdaş Ballı (e-mail: balli@ee.bilkent.edu.tr) and Abdullah Atalar are with the Department of Electrical and Electronics Engineering, Bilkent University, 06800 Ankara, Turkey.

Çağdaş Ballı, Ahmet Değirmenci, and Ahmet Aktuğ are with the Power Amplifiers and MMIC Design Department, Aselsan Inc., 06370 Ankara, Turkey.

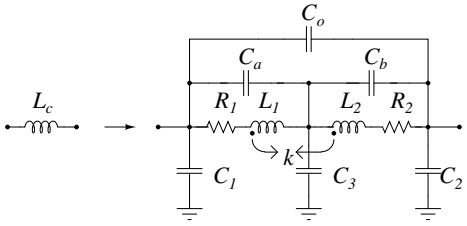

Fig. 3: Inductor model showing the parasitics.

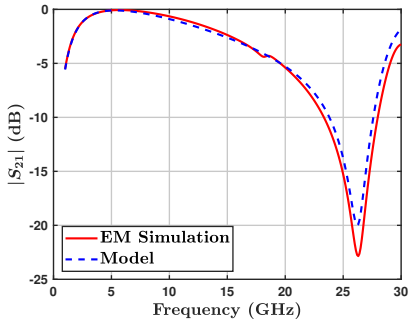

Fig. 4: Dashed line: $|S_{21}|$ as obtained from simulation of measured S-parameters of a shorted 2.7 nH inductor with a conductor width of $w_c = 60$ μm and parallel connected air bridges having a total width of 109 μm. Solid line: $|S_{21}|$ as obtained from the inductor's model with L_1=0.3 nH, L_2=1.9 nH, k=0.31, C_o+C_1=270 fF and C_a+C_b+C_3=190 fF.

and k is the coupling coefficient between the two coils given as

$$L_c = L_1 + L_2 + 2M \qquad M = k\sqrt{L_1 L_2} \tag{1}$$

The model parameters can be found with the aid of a CAD tool by fitting the measurement data. The loss and series resonance frequency (SRF) are easily seen as reductions or dips in $|S_{21}|$ as presented in Fig. 4. The figure also shows the calculated $|S_{21}|$ from the model parameters. The frequency of the SRF dip, f_s, observed in the figure can be found by:

$$f_s = \frac{1}{2\pi}\left(\frac{L_c}{(L_1L_2 - M^2)(C_a + C_b + C_3)}\right)^{1/2} \tag{2}$$

Clearly, $C_a + C_b + C_3$ is a critical parasitic factor.

From the simulation results of many spiral inductors [3], we find the series resonance frequency, f_s, as a function of conductor width, w_c (μm), and inductor value, L_c (nH) as

$$f_s \text{ (GHz)} \approx \frac{300}{w_c^{0.4} L_c^{0.8}} \text{ for } w_c < 60\mu\text{m} \tag{3}$$

Another source of loss at high frequencies is the total shunt parasitic capacitor of the inductor, $C_p = C_o + C_1$, which can be written for our process as

$$C_p \text{ (fF)} \approx 1.8 w_c^{0.9} L_c^{0.5} \text{ for } w_c < 23\mu\text{m} \tag{4}$$

For example, with w_c=18 μm and L_c=2.7 nH, f_s=35.5 GHz and C_p=40 fF with a current limit of I_c=0.35 A[4].

[3]For all inductors, the spacing between the conductors is 5 μm, the minimum value for the process technology.

[4]The current limit for air bridge metal is 23.44 mA/μm, and its width is 3 μm less than the conductor width w_c.

When $I_c > 0.35$ A, we must set $w_c > 23$ μm. In this case, the performance of the inductor degrades severely due to design rule limitations: There are current limits for a maximum width air bridge and the thinner metal underneath it. Hence several air bridges and undermetals need to be connected in parallel and consequently, C_p increases dramatically. For w_c = 60 μm, a current of 1.74 A is achievable with four parallel air bridges and seven parallel undermetals resulting in a footprint of 0.544 mm^2 and C_p=270 fF (see Fig. 4) C_p value is much higher than that is predicted from Eq. 4.

III. Distributed Choke Inductor

For high currents, we propose to use n separate low-current spiral inductors each with a line width $w_c < 23$ μm connected to different stages of the distributed amplifier as shown in Fig. 5. There is a need to increase the value of each

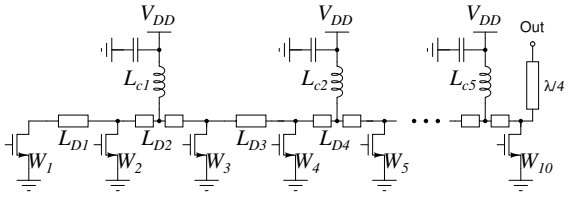

Fig. 5: Five spiral inductors placed on the drain line of a 10-stage NDPA with $W_1 = W_2 > W_3 = W_4 = ... = W_9 > W_{10}$.

inductor by a factor of k to keep the lower frequency limit the same. Fortunately, k is less than n due the presence of drain side inductors between stages contributing to the values of the choke inductors. Hence, the current carrying capacity is increased and the resistive loss in the drain bias is reduced.

A current limit of I_c=1.56 A [5] can be reached with n=5 inductors with w_c=18 μm each. In this case, each inductance should be increased to 4.8 nH ($k \approx$1.8, f_s=26.9 GHz, and C_p=53 fF). Since the inductors are placed in a distributed manner, C_ps can be used instead of the needed drain capacitors of an NDPA, eliminating the high-frequency gain degradation.

The calculated $|S_{21}|$ for a single inductor when $C_p = C_o + C_1$ is artificially removed from the model is shown in Fig. 6. As it can be seen, C_p influences the loss at the high-frequency side of the band. Elimination of C_p improves the performance at high frequencies.

A comparison of different choke inductor alternatives for an NDPA is simulated, and the results are presented in Fig. 7. If a single high-current L_c=2.7 nH spiral inductor with w_c=60 μm is used, less power is delivered at the high frequency end since its shunt capacitance is relatively large: C_p=270 fF. The performance of a commercial off-chip conical 425 nH 18 GHz inductor [6] is also shown. Since the current handling limit for this inductor is 1 A, two such inductors had to be used in parallel. As a result of the capacitance of the bonding pads, the performance at the high-frequency end degraded. As shown in the figure, the performance of the distributed inductor composed of five kL_c=4.8 nH low-current inductors with C_ps absorbed as part of the drain line is superior.

[5]It is less than 1.75 A due to unequal current division among inductors.

[6]CC21T36K240G5 from Piconics, Inc.

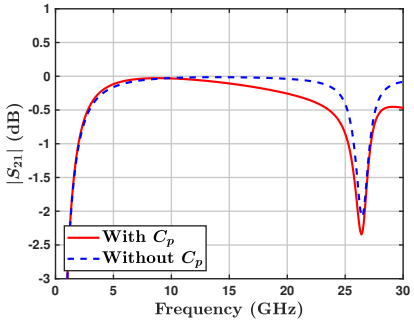

Fig. 6: $|S_{21}|$ simulation results with (solid) and without (dashed) C_p for a kL_c=4.8 nH inductor with $w_c = 18$ μm.

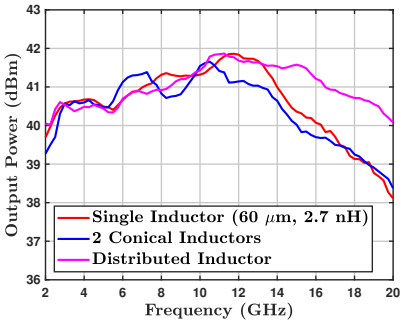

Fig. 7: Results of the harmonic balance simulation of the NDPA using different choke inductors.

IV. NDPA Design and Measurement Results

A 10-stage NDPA is designed using the method of [2] with a drain impedance of 35 Ω and a total gate width of 4.29 mm for the 0.25 μm GaN on SiC process (see Figs. 5 & 8). We obtain different characteristic impedances for each drain line, resulting in an efficient combination of transistor currents. NDPA has five kL_c=4.8 nH inductors (w_c=18μm, each with an area of 0.114 mm^2) placed in a distributed manner with three decoupling capacitors for each. The equivalent choke inductance of L_c=2.7 nH is capable of supplying a total current of 1.56 A. The equivalent DC resistance of the choke inductor (the total DC resistive loss in the drain bias network divided by the square of the DC bias current) is only 0.32 Ω.

On-wafer small-signal and large-signal measurements of the NDPA were done with a CW input. Fig. 9 and 10 depict the measured S-parameters, output power, and drain efficiency of the amplifier. The measured S-parameters shown in Fig. 9 compare well with the simulations. The output power varies between 39.0–41.7 dBm, and the power-added efficiency is greater than 20% over the 2–18 GHz frequency range. A comparison of our NDPA design with those given in the literature is presented in Table I. Our design has a comparable performance even though it uses a 0.25 μm process.

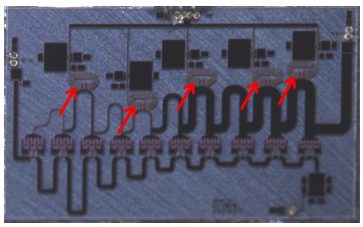

Fig. 8: Photo of the fabricated MMIC with inductors pointed.

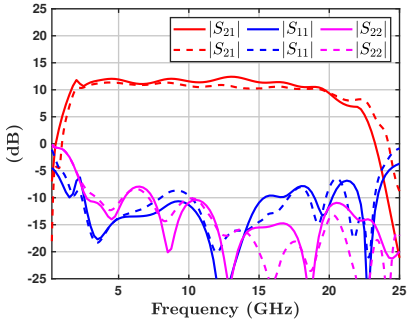

Fig. 9: Measured (dashed) and simulated (solid) S-parameters

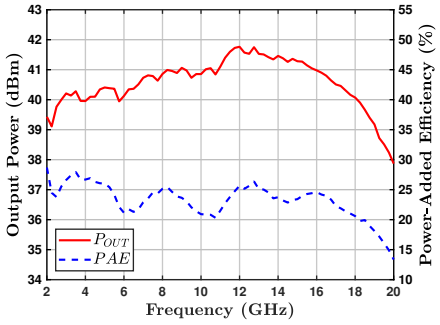

Fig. 10: On-wafer CW measured power and PAE of NDPA with V_{DD}=28 V, V_{GG}=−2.14 V, and I_Q=0.53 A.

V. Conclusions

The performance of a high-current on-chip choke inductor is degraded severely due to shunt parasitics of air bridges. We showed how such inductors can be implemented using a number of low-current inductors paralleled in a distributed manner to lower the DC resistive loss, eliminate the shunt parasitics, and enhance the high-frequency gain. The method can be used in all NDPA structures to improve the efficiency.

References	[2]	[5]	[7]	[12]	[8]	T.W.
Process (μm)	0.25	0.10	0.15	0.20	0.15	0.25
f (GHz)	2–18	2–18	2–20	0–20	2–20	2–18
S_{21} (dB)	10	28	19	12	17	10
P_{out} (W)	5.6–12.5	9.1–15.8	10.7–15.8	4	18–30.8	8–15
PAE (%)	15–35	18–38	22–38	10–15	18–29.7	20–28
V_{DD} (V)	30	28	22	30	22	28
Size (mm^2)	15.3	7	10.5	4.8	25.8	13.4

TABLE I: Comparison of the DPAs with GaN on SiC.

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